|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Operacion | RegDst | RegWrite | ALUSrc | ALUOp | MemWrite | MemRead | MemToReg |
| Add | 1 | 1 | 0 | 010 | 0 | 0 | 0 |
| Sub | 1 | 1 | 0 | 110 | 0 | 0 | 0 |
| Or | 1 | 1 | 0 | 001 | 0 | 0 | 0 |
| And | 1 | 1 | 0 | 000 | 0 | 0 | 0 |
| Slt | 1 | 1 | 0 | 111 | 0 | 0 | 0 |
| Lw | 0 | 1 | 1 | 010 | 0 | 1 | 1 |
| Sw | x | 0 | 1 | 010 | 1 | 0 | x |
| Beq | x | 0 | 0 | 110 | 0 | 0 | x |